SRI SIDDHARTHA INSTITUTE OF TECHNOLOGY, TUMAKURU

(A constituent college of Sri Siddhartha Academy of Higher Education, Tumakuru)

CS3TH5: Digital Circuit Design & Applications

Date:27/11/2021 **TEST 1** Time:1Hr

Max Marks: 30

Answer all the questions

		M	C	B
1	What are Maxterms? Convert the given Boolean expression to standard POS and later to Maxterm Canonical form (ii) $f(abc)= (\bar{a}+c) . (b + c)$ (ii) $f(abc)= \bar{c}$	6	1	2
2	Design one bit comparator using basic gates and NAND gates.	6	2	3
3	Write the Verilog code for the logic circuit which produces logic-1 output for even number of 1's for the set of 8 input combinations.	6	4	5
4	Design a Combinational logic circuit which accepts four input variables and produces logic-0 output for those input combinations which have two or more zeros. Use Minimum number of logic gates.	6	2	3
5.	Simplify the following expressions using K- map (iii) $f(abcd)= \Sigma m(1,3,4,6,10,11,15)$ (iv) $y(pqrs) = \pi M(0,2,5,6,8,9,12,14,)$ Write the logic circuit for the simplified expression using **universal gates**	6	2	4

NOTE: M -Marks, C- Course Outcome and B – Bloom's level

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Date:01/01/2022 **TEST 2** Time:1Hr

Answer all the questions } Max Marks: 30

		M	C	B
1	Design Adder / Subtractor circuit using 4 bit adder IC 7483 and write the single truth table to depict the addition and subtraction of following numbers. **(iv) A=6 & B= 2** **(v) A=7 & B=5** (vi) **A=4 & B=1**	6	2	6
2	Write the HDL code for 3:8 Decoder using Case statement	6	4	3
3	Realize the given Boolean Expression using suitable Multiplexer **F(ABCD)= $\sum$m(0,1,2,4,6,8,9,11,12,14,15)** **P(XYZ)= $\prod$ M(1,3,4,6)**	6	2,3	4,6
4	Write the Truth Table of BCD to 7 Segment decoder and obtain the Boolean expression for the segment **'d'**	6	2	5
5	Design a logic circuit which converts 2^3 decimal inputs to 3 bit Binary output	6	1,2	5,6

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Date:05/02/2022 **TEST - 3** Time:1Hr

Answer all the questions Max Marks: 20

		M	CO	BL
1	Explain the working of D Flip Flop and mention the merits of D Flip Flop	5	1	2
2	Obtain the characteristic equation of SR and JK Flip Flop	5	2	5
3	Convert SR flip flop to D Flip Flop	5	2,3	6
4	Design Mod 4 Synchronous up counter and write the Timing diagram	5	2	4

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